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for

Conditional Burn-In Keeper for Dynamic Circuits

by

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Field

[0001] Embodiments of the present invention relate to digital circuits, and more particularly, to dynamic circuits.

Background

[0002] The functionality and reliability of microprocessors are usually tested under conditions that are relatively extreme when compared to normal operating conditions. During testing, the temperature and supply voltage may exceed the upper bounds of their respective target operating ranges. This is often referred to as burn-in or stress testing.

[0003] The burn-in process may set a severe constraint on dynamic circuits, requiring relatively large keepers during burn-in to compensate for additional leakage currents due to the higher temperature and supply voltage. Leakage currents are relatively small currents present when a transistor is not fully turned ON, e.g., when the magnitude of the gate-to-source voltage is less than the transistor's threshold voltage. Leakage current may present more of a design problem as transistor sizes are made smaller. Although larger keepers may meet the burn-in condition while compensating for leakage currents in the dynamic circuit, they nevertheless would be oversized for normal operating conditions. Using larger keepers during normal operating conditions may degrade microprocessor performance.

[0004] The prior art circuit of Fig. 1 provides a conditional keeper for burn-in, and a normally sized keeper during normal operation, so that the burn-in conditions are met without degrading the performance of the microprocessor during normal operation. See D. Stasiak, et al., "A 2nd Generation 440ps SOI 64b Adder," ISSCC 2000, pp. 288-289.

[0005] For simplicity, only one stage of a dynamic circuit is shown in Fig. 1. Network **102** represents a plurality of nMOSFETs (Metal Oxide Semiconductor Field Effect Transistor) configured to conditionally pull node **110** LOW during an evaluation phase so as to synthesize the particular logic function that is desired. During an evaluation phase, pMOSFET **104** is OFF, and during a pre-charge phase, pMOSFET **104** is ON to pull node **110** HIGH. Network **102** in general will have a plurality of input ports for receiving digital voltages, perhaps from other stages in the dynamic circuit.

[0006] Inverter **106** and pMOSFET **108** are configured as a keeper (or half-keeper), so that during an evaluation phase node **110** is kept HIGH if network **102** does not pull node **110** LOW. Static CMOS (Complementary Metal Oxide Semiconductor) **116** may be a static inverter or other logic gate, whose output may be provided to another stage of the dynamic circuit.

[0007] Inverter **106** and pMOSFET **108** are sized for normal operating conditions. The two stacked pMOSFETs **112** and **114**, together with inverter **106**, comprise what may be referred to as a conditional keeper for burn-in testing. pMOSFETs **112** and **114** are sized appropriately for the operating conditions of a burn-in test. The gate of pMOSFET **114** is activated by a signal BI-active (Burn-In active), where BI-active is set HIGH when the microprocessor is operating normally, and is set LOW during a burn-in test. With BI-active set LOW, pMOSFET **114** is ON, and inverter **106**, together with pMOSFETs **112** and **114**, act as a keeper, properly sized for the burn-in conditions.

[0008] Stacking MOSFETs, i.e., connecting the drain of one to the source of the other, reduces their overall effective gain. Because pMOSFETs **112** and **114** are in a stacked configuration, they should be sized up approximately twice as large as compared for a single, non-stacked pMOSFET keeper in order to compensate for the reduced gain. However, sizing up pMOSFETs **112** and **114** may have some disadvantages. Sizing up pMOSFETs **112** and **114** uses a larger chip (die) area. Also, the larger size increases the load on inverter **106**, which may degrade the response of pMOSFET **108** when performing its standard keeper operation during normal operation conditions. As a result, inverter **106** may also need to be sized larger, which in turn increases the load on node **110**, which may result in an increase in switching power and delay of the dynamic gate.

Brief Description of the Drawings

[0009] Fig. 1 is a prior art circuit for a stage of a dynamic circuit with a conditional keeper for burn-in.

[0010] Fig. 2 is a stage of a dynamic circuit with a conditional keeper for burn-in according to an embodiment of the present invention.

Description of Embodiments

[0011] Fig. 2 is a circuit according to an embodiment of the present invention, where again for simplicity only one stage of a dynamic circuit is shown. Network **202**, pMOSFET **204**, and static CMOS **216** provide the same function as network **102**, pMOSFET **104**, and static CMOS **116**, respectively, in Fig. 1. Inverter **206** and pMOSFET **208** comprise a keeper to keep node **210** HIGH if it is not pulled LOW by network **202** during an evaluation phase. NAND gate **218** and pMOSFET **220** comprise a conditional keeper for burn-in. Input port **222** of NAND gate **218** is connected to node **210**, and input port **224** of NAND gate **218** is provided with a signal BI-active#, where BI-active# is the complement of BI-active, so that BI-active# is HIGH (BI-active is LOW) during a burn-in test, and BI-active# is LOW (BI-active is HIGH) during normal operation.

[0012] It is seen that during burn-in, pMOSFET **220** will also keep node **210** HIGH if it is not pulled LOW by network **202** during an evaluation phase. It is preferable that pMOSFET **220** should be sized so that the combination of pMOSFET **220** and pMOSFET **208** provides a sufficiently strong keeper to compensate for additional leakage currents due to burn-in testing.

[0013] For some embodiments, the size of pMOSFET **220** may be made four times smaller than the total size of pMOSFETs **112** and **114**, while still compensating for increased leakage currents during burn-in testing. The activation signal BI-active# may be viewed as a DC signal, so that it does not set a constraint on the size of NAND gate **218**. The size of NAND gate **218** is set by the target transient response for pMOSFET **220**, however for some embodiments pMOSFET **220** may be up to two times smaller than pMOSFET **114**. Thus, for some embodiments the total size of NAND gate **218** together with pMOSFET **220** is close to the size of inverter **106** in the prior art, and therefore the total area of the conditional keeper in Fig. 2 may be significantly less than that of the prior art.

[0014] Often, the burn-in process tests for reliability and functionality, rather than performance. Consequently, the dynamic circuit may be operated at a lower frequency during a burn-in test than when operated under normal operation conditions. In such cases, performance requirements may be relaxed during the burn-in test, so that the speed

and transient response of the conditional keeper may be relaxed as well. Therefore, in such cases, the size of NAND gate **218** may be reduced even further. Hence, for wide dynamic gates (e.g., large number of parallel paths in network **202**), the conditional keeper may result in less output load seen by node **210**. The lighter load may result in a higher performance for the dynamic circuit during normal operation conditions.

[0015] Many other embodiments of the invention than those described herein may be practiced, and many modifications may be made to the described embodiments, without departing from the scope of the invention as claimed below. For example, some pMOSFETs may be replaced with nMOSFETs, and BiCMOS (Bipolar CMOS) as well as other process technologies may be employed.